REMARKS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art. Claims 1, 12, 21, 24-26, 30, 36, 39, 45, and 48 have been amended. No claims have been added or cancelled. No new matter has been introduced as a result of these amendments.

The Examiner rejected claims 24-26 under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Applicants amended the claim 24-26 to recite an "article of manufacture comprising the machine readable storage medium" (*See* claims 24-26). Because the Applicants claim a machine readable storage medium that "require[s] physical substance, which a claimed signal does not have" (*See* "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility"), Applicants respectfully submit that claims 24-26 satisfy the requirements of § 101 and the interim guidelines. Thus, Applicant requests withdrawal of the rejections under 35 U.S.C. § 101.

The Examiner rejected claims 1, 4, 7-14, 17-26, 29, 30, 34-36, 48, 52, and 53 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,816,961 of Rice et al. (hereinafter referred to as "Rice") in view of Goodman & Miller, "A Programmer's View of Computer Architecture" (hereinafter referred to as "Goodman"). Applicants respectfully disagree because the references, alone or in combination, fail to describe each and every element of the invention as claimed.

Rice describes a system that swaps bytes by selecting which field in a destination register receives which field from a source register (Rice, column 2, lines 45-51). Specifically, Rice describes a source register that includes a plurality of operation fields

(Rice, column 2, lines 1-10). The fields contain two parts, a 3-bit portion and 5-bit codes that trigger the various operations (*See* Rice, column 8, Table II). Rice explicitly teaches that "five bits [are] devoted to the operation field" where a 5-bit sequence determines what operation is to be performed (Rice, column 7, lines 51-53).

Goodman describes instruction formats (Goodman, page 199). Goodman describes, at only a very high level, that a two address format for an instruction specifies that an address may act as both an addend and the address for storing a result (Goodman, page 199).

In amended claim 1, the Applicants recite:

> A method comprising:
> responsive to receiving a single packed shuffle instruction designating, with 3 bits, a first register storing a first operand having a set of L data elements and designating, with 3 bits, a second register storing a second operand having a set of L control elements, wherein the first operand and second operand are of a same size and each of the L data elements and L control elements are of a same size, and wherein each one of the L control elements is divided into three portions, the first portion being a flush to zero bit occupying the most significant bit of each control element wherein the flush to zero bit alone controls whether a resultant element is flushed to zero, the second portion being a position selection field that is at least $\log_2 L$ bits wide and indicates a position of one of said L data elements, and a third portion, storing a resultant operand in said first register having L resultant data elements of the same size as the L data elements and the L control elements, wherein the value of each resultant data element is controlled by the position selection field of the L control elements in the same position as the resultant data element, and is either,
> the one of the L data elements designated by the position selection field of said control element if said control element's flush to zero bit is not set; or
> a zero if said control element's flush to zero bit is set.
> (emphasis added)

The Applicants respectfully submit that Rice and Goodman, alone or in combination, fail to describe each and every feature as claimed in claim 1.

The Examiner noted in the Advisory Action (mailed 12/19/06) that Rice describes an operation field that includes a bit which operates "in conjunction with other bits" (See Advisory Action, page 2). The Applicants now claim in amended claim 1 a control element where "the first portion [of the control element] being a flush to zero bit occupying the most significant bit of the control element wherein the flush to zero bit alone controls whether a resultant element is flushed to zero" (emphasis added). Because the "flush to zero bit alone controls whether a resultant element is flushed to zero," as claimed by the Applicants, does not operate in conjunction with other bits of the control element, Rice fails to make obvious each and every feature claimed by the Applicants.

The Examiner stated that the operation field is divided into two portions, where the "least significant bit is a flush to zero bit" (Final Office Action, page 4 *citing* Rice at Table I). However, Table I of Rice shows that the five-bit operation field is not divisible as argued by the Examiner. In particular, the Applicants point the Examiner's attention to operation field "00001" which results in "each bit from the source field [set] low", in contrast to "01001" which would result in "each bit of the source field [set] high" (Rice Table I). As such, the least significant bit of Rice's control field serves no special purpose. In fact, the same value in the least significant field of Rice leads to exactly the opposite result. Thus, Rice describes utilizing the entire indivisible 5-bits "dedicated to" the operation field to define particular operations.

Furthermore, because Rice dedicates two fields to the byte swap operation, Rice must fail to describe or suggest a three-portion control element, where the third portion is not a mask field and not a zero flag field.

The Examiner further states that:

> [I]t would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the operation field codes so that the code "10000" indicates the operation currently performed when th code "00001" and vice versa ... because Applicant has not disclosed that the flush to zero bit occupying the most significant bit of each control element provides an advantage, is used for a particular purpose, or solves a stated problem. (Final Office Action, page 5).

However, the Applicants submit that the claimed configuration is not a "matter of design choice" as asserted by the Examiner. The Applicants' specification recites "the 'set to zero flag' field is dominant wherein if the 'set to zero flag' field 315 is set, the rest of the fields in the mask 318 are ignored and the resultant data element position is filled with '0'" (Specification as originally filed, Paragraph [0073]). As the specification indicates, by using a flush to zero flag (i.e., the MSB), the remainder of the fields may be ignored without requiring the processing of such fields. Thus, in contrast to the assertions of the Examiner, the claimed configuration is utilized for a particular purpose, which advantageously avoids unnecessarily processing data when a flush to zero has been detected.

As noted above, Goodman merely provides a high level discussion of various computer architecture instruction formats (*See* Goodman, pages 199-202). As such, Goodman is silent as to the limitations and features discussed above.

Therefore, the Applicants respectfully submit that Goodman and Rice, alone or in combination, fail to describe or suggest each and every element of claim 1. Thus, claim 1 is not rendered obvious by Rice in view of Goodman, for at least the reasons noted above. Furthermore, claims 4, 7-14, 17-26, 29, 30, 34-36, 48, 52, and 53 contain similar features and limitations to those discussed above with respect to claim 1. Thus, for similar

reasons, claims 4, 7-14, 17-26, 29, 30, 34-36, 48, 52, and 53 are also not rendered obvious by Rice in view of Goodman, for similar reasons to those advanced with respect to claim 1. Therefore, the Applicant respectfully requests withdrawal of the rejections of claim 1, 4, 7-14, 17-26, 29, 30, 34-36, 48, 52, and 53under 35 U.S.C. § 103(a), and submit that the claims are in condition for allowance.

The Examiner rejected claims 39-47 under 35 U.S.C. § 103(a) as being unpatentable over Rice and Goodman, in view of U.S. Patent Application Publication 2005/0188182 of Hoyle et al. (hereinafter "Hoyle"). Similar to the discussion above, with respect to independent claim 1, Rice and Goodman, alone or in combination, similarly fails to describe or suggest each and every element of amended independent claims 39 and 45. Hoyle discusses a system where instructions perform byte intermingling from two source operands and store a result in a third result operand (Hoyle, Abstract). Because the various three-operand byte intermingling instructions merely perform predefined intermingling operations (*See* Hoyle, Table 9), Hoyle similarly fails to teach or suggest the limitations noted above. Therefore, for reasons similar to those discussed with respect to claim 1, Rice, Goodman, and Hoyle, alone or in combination fail to describe or suggest the limitations recited in claims 39 and 45, along with their respective dependent claims. The Applicants therefore respectfully request withdrawal of the rejections.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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Date: 12/20/06

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